REMARKS/ARGUMENTS

The present Amendment is in response to the Office Action mailed November 15, 2002 in the above-identified patent application. Enclosed herewith is a Petition requesting a three-month extension of time for resetting the deadline for responding to the Office Action from February 15, 2003, to and including May 15, 2003.

As an initial matter, Applicants acknowledge and appreciate the Examiner's indication that claims 26-39 are allowed and that claims 3, 8-9, 13-19 and 25 would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

The Examiner rejected claims 1, 11-12, 20, 22 and 24 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 4,818,728 to *Rai et al.* Referring to FIGS. 1(A)-1(C) thereof, *Rai* discloses a method of electrically interconnecting two semiconductor devices including a first semiconductor device 1 having electrodes 2, an insulating layer 3 and metal studs 4 made of copper or gold. A second semiconductor device 1' includes electrodes 2', insulating layer 3' and solder deposits 5 made of, for example, Sn, Pb or In. Referring to FIG. 1(C), during assembly, the metal studs 4 of first semiconductor device 1 are aligned with electrodes 2' and solder deposits 5 of second semiconductor device 1'. The solder deposits are heated and the metal studs 4 are pressed into the melted solder deposits 5 for creating an electrical interconnection between the first semiconductor device 1 and the second semiconductor device 1'. Applicants respectfully assert that the claims of the present application are substantially different than what is disclosed in *Rai* because the claims require that the microelectronic assembly be tested while a second fusible material is maintained in a molten or a liquid state. In response to the Examiner's

rejection, claim 1 has been amended as indicated above. Claim 1 is unanticipated by *Rai* because the cited reference does not disclose a method of making a microelectronic assembly including "testing said microelectronic assembly after the electrically interconnecting step while maintaining said second fusible material at a temperature that is greater than or equal to the second melting temperature." For all of these reasons, claim 1 is unanticipated by *Rai* and is otherwise allowable. Claims 11-12, 20, 22 and 24 are also unanticipated, *inter alia,* by virtue of their dependence from claim 1, which is unanticipated for the reasons set forth above.

The Examiner also rejected claims 2, 4-7 and 10 under 35 U.S.C. § 103(a) as being unpatentable over *Rai* in view of U.S. Patent 6,288,559 to *Bernier et al.* Referring to FIG. 5 thereof, *Bernier* teaches a method for testing and burning-in of semiconductor circuits that permits an entire wafer to be tested by temporarily attaching the wafer to a test substrate using electrically conductive adhesive (ECA). Referring to FIG. 5, to test an entire wafer 30, an alignment is performed between wafer 30 and test substrate 36. Bumps made of electrically conductive adhesive 33 conform to the variances in chip wafer pads 32 and substrate test pads 35. After testing is completed, a solvent is applied to dissolve and remove the ECA material from the wafer 30. As a result, removal of the test wafer 30 from the test substrate 36 is possible. Although *Bernier* teaches using an electrically conductive adhesive, the adhesive is not a "second fusible material having a second melting temperature that is lower than the first melting temperature of said first fusible material." Moreover, *Bernier* does not overcome the deficiencies noted above in *Rai*. For all of these reasons, claims 2, 5-7 and 10 are unobvious over *Rai* and *Bernier* and are otherwise allowable. Claims 2, 5-7 and 10 are also allowable,

inter alia, by virtue of their dependence on claim 1, which is allowable for the reasons set forth above.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

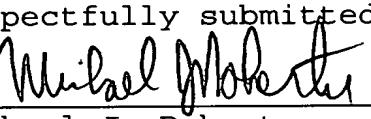
As it is believed that all of the rejections set forth in the Official Action have been fully met, favorable reconsideration and allowance are earnestly solicited.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he telephone Applicants' attorney at (908) 654-5000 in order to overcome any additional objections which he might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

Dated: April 30, 2003

Respectfully submitted,

By 

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Version With Markings to Show Changes Made

IN THE ABSTRACT

A method of making a microelectronic assembly includes providing a first microelectronic element having one or more conductive bumps, the conductive bumps including a first fusible material that transforms from a solid to a liquid at a first melting temperature, and providing a second microelectronic element having one or more conductive elements. The conductive bumps of the first microelectronic element are electrically interconnected with the conductive elements of the second microelectronic element using a second fusible material, the second fusible material having a second melting temperature that is lower than the first melting temperature of the first fusible material. During the electrically interconnecting step, the second fusible material is maintained at a temperature that is greater than or equal to the second melting temperature and less than the first melting temperature of the first fusible material. The method also includes testing the microelectronic assembly after the electrically interconnecting step while maintaining the second fusible material at a temperature that is greater than or equal to the second melting temperature.

IN THE CLAIMS

1. (Amended) A method of making a microelectronic assembly comprising:

providing a first microelectronic element having one or more conductive bumps, said conductive bumps including a first fusible material that transforms from a solid to a liquid at a first melting temperature;

providing a second microelectronic element having one or more conductive elements;

electrically interconnecting said conductive bumps of said first microelectronic element and said conductive elements of said second microelectronic element using a second fusible material, said second fusible material having a second melting temperature that is lower than the first melting temperature of said first fusible material; ~~and~~

during the electrically interconnecting step, maintaining said second fusible material at a temperature that is greater than or equal to the second melting temperature and less than the first melting temperature of said first fusible material~~.~~; and

testing said microelectronic assembly after the electrically interconnecting step while maintaining said second fusible material at a temperature that is greater than or equal to the second melting temperature.

5. (Amended) The method as claimed in claim 4~~1~~, further comprising lowering the temperature of said second fusible material to a temperature that is less than the second melting temperature.

8. (Amended) The method as claimed in claim 4~~1~~, further comprising after the testing step, raising the temperature of the first fusible material to a temperature that is greater than the first melting temperature of said first fusible material for mixing the first and second fusible materials together to form one or more conductive masses.

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